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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/004,458	10/23/2001	Thomas Fung	2875.0440001	6843
26111	7590	02/17/2009	EXAMINER	
STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.			POPHAM, JEFFREY D	
1100 NEW YORK AVENUE, N.W.				
WASHINGTON, DC 20005			ART UNIT	PAPER NUMBER
			2437	
			MAIL DATE	DELIVERY MODE
			02/17/2009	PAPER

**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

<b>Office Action Summary</b>	<b>Application No.</b>	<b>Applicant(s)</b>	
	10/004,458	FUNG ET AL.	
	<b>Examiner</b>	<b>Art Unit</b>	
	JEFFREY D. POPHAM	2437	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

#### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

#### Status

1) Responsive to communication(s) filed on 24 November 2008.  
 2a) This action is **FINAL**.                    2b) This action is non-final.  
 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

#### Disposition of Claims

4) Claim(s) 1-4,8-12,14-18,20-24 and 26 is/are pending in the application.  
 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.  
 5) Claim(s) \_\_\_\_\_ is/are allowed.  
 6) Claim(s) 1-4,8-12,14-18,20-24 and 26 is/are rejected.  
 7) Claim(s) \_\_\_\_\_ is/are objected to.  
 8) Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

#### Application Papers

9) The specification is objected to by the Examiner.  
 10) The drawing(s) filed on 01 September 2005 is/are: a) accepted or b) objected to by the Examiner.  
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).  
 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

#### Priority under 35 U.S.C. § 119

12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).  
 a) All    b) Some \* c) None of:  
 1. Certified copies of the priority documents have been received.  
 2. Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.  
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

#### Attachment(s)

1) <input type="checkbox"/> Notice of References Cited (PTO-892)	4) <input type="checkbox"/> Interview Summary (PTO-413)
2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)	Paper No(s)/Mail Date. _____ .
3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)	5) <input type="checkbox"/> Notice of Informal Patent Application
Paper No(s)/Mail Date _____.	6) <input type="checkbox"/> Other: _____ .

***Remarks***

Claims 1-4, 8-12, 14-18, 20-24, and 26 are pending.

***Response to Arguments***

1. Applicant's arguments filed 11/24/2008 have been fully considered but they are not persuasive.

Applicant argues that Nakaya does not teach disabling a first interrupt indicator associated with the first data, when the processing of the first data completes before the processing of the second data, or enabling a second interrupt indicator associated with the second data, when the processing of the first data completes before the processing of the second data. As noted in the previous rejection of claim 1, Nakaya does not explicitly disclose the enablement of a first interrupt indicator. Furthermore, with respect to the limitations discussed, Nakaya does disclose moving a first interrupt indicator associated with a younger control record onto a second interrupt indicator associated with an older control record if processing of the first data completes before processing of the second data. As further discussed in claim 4, dependent from claim 1, "moving the first interrupt indicator comprises delaying the generation of an interrupt with the younger control record." Since Applicant has noted that Nakaya "discloses parallel computer parts that delay the issuance of an interrupt until all of the multiple parallel computer parts (e.g., U2 through U6) are finished", one will readily see that Nakaya discloses moving an interrupt indicator onto another, wherein such moving comprises delaying the generation of an interrupt.

Applicant goes on to argue that Yamaura and Ghaffari are silent with respect to processing first and second data in respective processing engines and, therefore, cannot teach the limitations noted above. As seen from the combination as a whole, Nakaya teaches processing of first and second data in respective processing engines, and this is not argued. Yamaura teaches the enabling and disable of interrupt indicators that can be used in the combination for the moving described within Nakaya. Ghaffari discusses further data that can be seen as a modification of the interrupt indicators of Nakaya-Yamaura, or additional interrupt indicators to be used within the system, such as the command chaining field that can be enabled or disabled in order to either provide an interrupt after command completion or wait until other commands are completed before providing such an interrupt, and issuing a single interrupt at the completion of all commands in the set. As one can see, the combination, as a whole, teaches disabling a first interrupt indicator associated with the first data, when the processing of the first data completes before the processing of the second data, or enabling a second interrupt indicator associated with the second data, when the processing of the first data completes before the processing of the second data, even though no single reference may teach the entirety of the limitations.

At the bottom of page 11, Applicant states that “dependent claims 17, 20, and 21 have been cancelled by the above amendment”, however, they still appear in the amended claims. The Examiner is unsure if these claims are supposed to be cancelled or not, but they are rejected below as they are still within the amended set of claims.

***Claim Objections***

2. Claims 1 and 15 are objected to because of the following informalities:

Claim 1 refers to "the younger control record" in the second to last limitation, however, there are 2 younger control records discussed in the claim and it is unclear which these references are referring to. Claim 1 refers to both "processing first data associated with a younger control record" and "enabling a first interrupt indicator in a younger control record". These appear to be separate instances of younger control records, based on the "a" language before them, but it is unclear how they differ and which one is being referred to later on, and it appears as though they should be the same control record. For purposes of prior art rejection, these have all been construed as the same control record.

Claim 15 refers to "the younger control record" and "the older control record" in the final limitation, but neither of these have been discussed previously in the claim. The correlation between younger/older and first/second has to be made clear. For purposes of prior art rejection, the younger control record has been construed as being the first control record and the older control record has been construed as being the second control record.

Appropriate correction is required.

***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

3. Claims 1, 3, 4, 8-12, and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nakaya (U.S. Patent 5,978,830) in view of Yamaura (U.S. Patent 6,175,890) and Ghaffari (U.S. Patent 6,145,017).

Regarding Claim 1,

Nakaya discloses a method for processing data using a plurality of processing engines, the method comprising:

Processing first data associated with a younger control record in a first processing engine (Figure 7; Column 12, lines 10-62; and Column 25, line 40 to Column 26, line 12);

Processing second data associated with an older control record in a second processing engine (Figure 7; Column 12, lines 10-62; and Column 25, line 40 to Column 26, line 12);

If processing of the first data completes before processing of the second data, moving a first interrupt indicator associated with the younger control record onto a second interrupt indicator associated with the older control record (Figure 7; Column 12, lines 10-62; and Column 25, line 40 to Column 26, line 12); and

If processing of the first data completes after processing of the second data, generating an interrupt when processing of the

first data completes (Figure 7; Column 12, lines 10-62; and Column 25, line 40 to Column 26, line 12);

But does not explicitly disclose enabling a first interrupt indicator in a younger control record, or that moving the first interrupt indicator comprises setting the first interrupt indicator associated with the younger control record to disabled and setting the second interrupt indicator associated with the older control record to enabled.

Yamaura, however, discloses enabling a first interrupt indicator in a younger control record; and that moving the first interrupt indicator comprises setting the first interrupt indicator associated with the younger control record to disabled and setting the second interrupt indicator associated with the older control record to enabled (Column 1, lines 12-30; and Column 4, line 59 to Column 5, line 10). Where the interrupt is placed, whether it be in a register devoted to interrupt indicators and their associations to control records or within the control record itself, is of no significance to this method, since placing the interrupt indicator within the control record does not provide an advantage over using a register to store the indicator. It would have been obvious to one of ordinary skill in the art at the time of applicant's invention to incorporate the interrupt handling method of Yamaura into the

parallel job scheduling system of Nakaya in order to efficiently restore data to be communicated to an external processor.

Ghaffari, however, discloses the enablement and disablement of interrupt indicators in order to provide for the issuing of interrupts only after particular sets of commands have completed processing; and if processing of first data completes after processing of second data, generating an interrupt when processing of the first data completes (Column 9, lines 3-25; and Column 10, lines 36-56). It would have been obvious to one of ordinary skill in the art at the time of applicant's invention to incorporate the control flags/fields of Ghaffari into the parallel job scheduling system of Nakaya as modified by Yamaura in order to explicitly designate whether an interrupt must be issued after completion of each command, so as to provide control over the frequency of command completion interrupts and thereby reduce the number of such interrupts issued and/or to tell the interrupt issuing entity that there are more commands to be executed before issuing the interrupt.

Regarding Claim 3,

Nakaya as modified by Yamaura and Ghaffari discloses the method of claim 1, in addition, Yamaura discloses that moving the first interrupt indicator comprises determining that the first interrupt

indicator is enabled (Column 1, lines 12-30; and Column 4, line 59 to Column 5, line 10).

Throughout this action, when the moving (or collapsing) of interrupt indicators is cited as being in Yamaura, it is to be understood that Yamaura teaches the foundations of how it is done, via the enabling and disabling of interrupt indicators within the interrupt controller, while the portions of Nakaya cited above discloses the moving of interrupt indicators (not issuing an interrupt until termination notices from all of the processors are issued).

Regarding Claim 4,

Nakaya as modified by Yamaura and Ghaffari discloses the method of claim 1, in addition, Nakaya discloses that moving the first interrupt indicator comprises delaying the generation of an interrupt associated with the younger control record (Column 25, lines 40-63). The termination notices are issued at all of the processors before any one of the processors can generate the interrupt.

Regarding Claim 8,

Nakaya as modified by Yamaura and Ghaffari discloses the method of claim 1, in addition, Nakaya discloses that the older control record comprises a reference to data (Column 12, lines 13-29).

Regarding Claim 9,

Nakaya as modified by Yamaura and Ghaffari discloses the method of claim 8, in addition, Nakaya discloses that the older control record comprises a reference to an operation to be performed on data (Column 12, lines 13-29).

Regarding Claim 10,

Nakaya as modified by Yamaura and Ghaffari discloses the method of claim 1, in addition, Yamaura discloses writing processed data to memory associated with a host (Column 4, line 59 to Column 5, line 49).

Regarding Claim 11,

Nakaya as modified by Yamaura and Ghaffari discloses the method of claim 10, in addition, Nakaya discloses that the processing engines are coupled to the interrupt controller (Figure 1); and Yamaura discloses that the external processor is coupled to the interrupt controller (Figure 1).

Regarding Claim 12,

Nakaya as modified by Yamaura and Ghaffari discloses the method of claim 11, in addition, Nakaya discloses that the external processor is coupled to the processing engines through a scheduler (synchronizer) (Figure 1).

Regarding Claim 14,

Nakaya as modified by Yamaura and Ghaffari discloses the method of claim 12, in addition, Yamaura discloses that the

external processor reads the processed data when the interrupt is generated (Column 4, line 59 to Column 5, line 49).

4. Claims 2, 15-18, 20-24, and 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nakaya in view of Yamaura and Ghaffari, further in view of Pierson (Pierson et al., "Context-Agile Encryption for High Speed Communication Networks", Computer Communications Review, Association for Computing Machinery, Vol. 29, No. 1, January 1999, pp. 35-49).

Regarding Claim 2,

Nakaya as modified by Yamaura and Ghaffari does not explicitly disclose that the first processing engine is a public key engine.

Pierson, however, discloses that the first processing engine is a public key engine (Pages 46-48, Section 5.2). It would have been obvious to one of ordinary skill in the art at the time of applicant's invention to incorporate the cryptographic system of Pierson into the parallel job scheduling system of Nakaya as modified by Yamaura and Ghaffari in order to allow the system to perform encryption and authentication quickly and easily, encrypting multiple communications (with different keys, algorithms, etc.) at a time without the normal delay required for context switching.

Regarding Claim 15,

Nakaya discloses an apparatus comprising:

A first processing engine configured to receive a first control record (Column 12, lines 10-62; and Column 25, line 40 to Column 26, line 12);

A second processing engine configured to receive a second control record (Column 12, lines 10-62; and Column 25, line 40 to Column 26, line 12);

A history buffer (interrupt controller/synchronizer) containing information associated with the first and second control records including a first interrupt indicator associated with the first control record and a second interrupt indicator associated with the second control record (Column 12, lines 10-62; and Column 25, line 40 to Column 26, line 12);

Wherein the history buffer is configured to move the first interrupt indicator associated with the first control record onto a second interrupt indicator associated with the second control record if processing of the first control record completes before processing of the second control record (Column 12, lines 10-62; and Column 25, line 40 to Column 26, line 12);

Wherein an interrupt is generated when processing of the first control record completes after processing of the second control record (Figure 7; Column 12, lines 10-62; and Column 25, line 40 to Column 26, line 12);

But does not explicitly disclose that the apparatus is a cryptography accelerator, an interface coupled to an external processor and memory associated with the external processor, or that moving the first interrupt indicator comprises setting the first interrupt indicator associated with a younger control record to disabled and setting the second interrupt indicator associated with an older control record to enabled.

Yamaura, however, discloses an interface coupled to an external processor and memory associated with the external processor; the interface being coupled to the processing engines as well; and that moving the first interrupt indicator comprises setting the first interrupt indicator associated with a first control record to disabled and setting the second interrupt indicator associated with a second control record to enabled (Column 1, lines 12-30; Column 4, line 59 to Column 5, line 10; and Figure 1). It would have been obvious to one of ordinary skill in the art at the time of applicant's invention to incorporate the interrupt handling method of Yamaura into the parallel job scheduling system of Nakaya in order to efficiently restore data to be communicated to an external processor.

Ghaffari, however, discloses that an interrupt is generated when the processing of the first control record completes if processing of the first control record completes after processing of

the second control record (Column 9, lines 3-25; and Column 10, lines 36-56). It would have been obvious to one of ordinary skill in the art at the time of applicant's invention to incorporate the control flags/fields of Ghaffari into the parallel job scheduling system of Nakaya as modified by Yamaura in order to explicitly designate whether an interrupt must be issued after completion of each command, so as to provide control over the frequency of command completion interrupts and thereby reduce the number of such interrupts issued and/or to tell the interrupt issuing entity that there are more commands to be executed before issuing the interrupt.

Pierson, however, discloses that the apparatus is a cryptography accelerator (Pages 46-48, Section 5.2). It would have been obvious to one of ordinary skill in the art at the time of applicant's invention to incorporate the cryptographic system of Pierson into the parallel job scheduling system of Nakaya as modified by Yamaura and Ghaffari in order to allow the system to perform encryption and authentication quickly and easily, encrypting multiple communications (with different keys, algorithms, etc.) at a time without the normal delay required for context switching.

Regarding Claim 16,

Nakaya as modified by Yamaura, Ghaffari, and Pierson discloses the apparatus of claim 15, in addition, Pierson discloses

that the first processing engine is a public key engine (Pages 46-48, Section 5.2).

Regarding Claim 17,

Nakaya as modified by Yamaura, Ghaffari, and Pierson discloses the apparatus of claim 15, in addition, Nakaya discloses that the history buffer is configured to collapse the first interrupt indicator associated with the first control record onto the second interrupt indicator associated with the second control record (Column 12, lines 10-62; and Column 25, line 40 to Column 26, line 12); and Yamaura discloses that this is performed when the first interrupt indicator is enabled (Column 1, lines 12-30; and Column 4, line 59 to Column 5, line 10).

Regarding Claim 18,

Nakaya as modified by Yamaura, Ghaffari, and Pierson discloses the apparatus of claim 17, in addition, Nakaya discloses that collapsing the first interrupt indicator associated with the first control record onto the second control record further comprises delaying the generation of an interrupt associated with the first control record (Column 12, lines 10-62; and Column 25, line 40 to Column 26, line 12).

Regarding Claim 20,

Nakaya as modified by Yamaura, Ghaffari, and Pierson discloses the apparatus of claim 18, in addition, Yamaura discloses

that collapsing the first interrupt indicator associated with the first control record onto the second control record further comprises setting the first interrupt indicator associated with the first control record to disabled (Column 1, lines 12-30; and Column 4, line 59 to Column 5, line 10).

Regarding Claim 21,

Nakaya as modified by Yamaura, Ghaffari, and Pierson discloses the apparatus of claim 20, in addition, Yamaura discloses that collapsing the first interrupt indicator associated with the first control record onto the second control record further comprises setting the second interrupt indicator associated with the second control record to enabled (Column 1, lines 12-30; and Column 4, line 59 to Column 5, line 10).

Regarding Claim 22,

Nakaya as modified by Yamaura, Ghaffari, and Pierson discloses the apparatus of claim 15, in addition, Nakaya discloses that the second control record comprises a reference to data (Column 12, lines 13-29).

Regarding Claim 23,

Nakaya as modified by Yamaura, Ghaffari, and Pierson discloses the apparatus of claim 22, in addition, Nakaya discloses that the second control record comprises a reference to an operation to be performed on data (Column 12, lines 13-29).

Regarding Claim 24,

Nakaya as modified by Yamaura, Ghaffari, and Pierson discloses the apparatus of claim 23, in addition, Nakaya discloses that the external processor is coupled to the processing engines through a scheduler (synchronizer) (Figure 1).

Regarding Claim 26,

Nakaya as modified by Yamaura, Ghaffari, and Pierson discloses the apparatus of claim 24, in addition, Yamaura discloses that the external processor reads the processed data when the interrupt is generated (Column 4, line 59 to Column 5, line 49).

### ***Conclusion***

**THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to JEFFREY D. POPHAM whose telephone number is (571)272-7215. The examiner can normally be reached on M-F 9:00-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Emmanuel Moise can be reached on (571)272-3865. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Jeffrey D Popham  
Examiner  
Art Unit 2437

/Jeffrey D Popham/  
Examiner, Art Unit 2437

/Emmanuel L. Moise/

